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T. BELL
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): M. OGINO

Serial No.: 09/429,297

Filed: October 28, 1999

For: SEMICONDUCTOR DEVICE, SEMICONDUCTOR WAFER, SEMICONDUCTOR MODULE, AND A METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

Group: 2822

Examiner: J. Mitchell

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

March 13, 2002

Sir:

In response to the Office Action mailed September 13, 2001, please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel claims 1, 7, 8, 15 and 16 without prejudice or disclaimer, and amend the claims remaining in the application as follows:

2. (Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to said stress relaxing layer of said semiconductor chip, and

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed outside of the semiconductor device on a same plane.

3. (Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

via-holes provided between the electrodes on said semiconductor chip and said circuit layer,

conductive portions for connecting electrically said circuit layer and

said electrodes in said via-holes,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane where the circuits and electrodes of said semiconductor chip are formed, wherein

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed outside of the semiconductor device on a same plane.

4. (Amended) A semiconductor device as claimed in claim 2 or 3, wherein

said organic protecting film has a linear expansion coefficient equivalent to the linear expansion coefficient of said stress relaxing layer.

9. (Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

anisotropic conductive material for connecting electrically said circuit layer and said electrodes on said semiconductor chip,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane, where the circuits and electrodes of said semiconductor chip are formed, wherein

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed outside of said semiconductor device on a same plane.

10. (Twice Amended) A semiconductor wafer comprising:

a chip for forming a semiconductor device, having a plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane of said chip, whereon the circuits and the electrodes are formed,

a circuit layer provided on said stress relaxing layer, and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to the plane, whereon said porous stress relaxing layer is provided, of said chip, and

side planes of the stress relaxing layer are exposed to outside of the semiconductor device.

11. (Twice Amended) A semiconductor wafer comprising:

a chip for forming a semiconductor device, having a plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane of said chip, whereon the circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer,

via-holes provided between said electrodes and said circuit layer,

conductive portions for electrically connecting said circuit layer and said electrodes in said via-holes,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane, opposite to the stress relaxing layer, of said chip,

wherein side planes of the stress relaxing layer are exposed to outside of the semiconductor device.

17. (Twice Amended) A semiconductor wafer comprising:

a chip for forming a semiconductor device, having a plurality of

chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane of said chip, whereon the circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer,

anisotropic conductive material for connecting electrically electrodes on a chip and a circuit layer,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane, whereon said circuits and electrodes are formed, of said chip,

wherein side planes of the stress relaxing layer are exposed to outside of the semiconductor device.

20. (Amended) A semiconductor module mounted with plurality of semiconductor devices as claimed in any one of claims 2 to 6 and 9.

Please add the following new claims to the application:

--21. A semiconductor device as claimed in any one of claims 2, 3 and 9, wherein said side planes of the stress relaxing layer, the semiconductor chip and the organic protecting film respectively form peripheral edges of the stress

relaxing layer, the semiconductor chip and the organic protecting film.

22. A semiconductor wafer as claimed in any one of claims 10, 11 and 17, wherein said side plane of the stress relaxing layer forms a peripheral edge thereof.

23. A semiconductor device as claimed in any one of claims 2, 3 and 9, wherein said stress relaxing layer is adhered to the semiconductor chip by an adhesion layer, and a linear expansion coefficient of the organic protecting film is substantially equivalent to the linear expansion coefficient of said adhesion layer.

24. A semiconductor device as claimed in claim 4, wherein said stress relaxing layer is adhered to the semiconductor chip by an adhesion layer, and a linear expansion coefficient of the organic protecting film is substantially equivalent to the linear expansion coefficient of said adhesion layer.

25. A semiconductor device as claimed in any one of claims 2, 3 and 9, wherein said porous stress relaxing layer has a greater porosity than that of the organic protecting film.

26. A semiconductor device as claimed in any one of claims 2, 3 and 9, wherein the organic protecting film is colored black.--

REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended claims 2, 3 and 9 to further clarify that respective side planes of the stress relaxing layer, semiconductor chip and organic protecting film are exposed outside "of said semiconductor device", on a same plane. Claims 10, 11 and 17 have been amended to recite that the wafer includes a chip for forming a semiconductor device, and to recite that side planes of the stress relaxing layer are exposed to outside of the semiconductor device. Claim 10 has been further amended to recite a "porous" stress relaxing layer.

In addition, claims 1, 7, 8, 15 and 16 have been canceled without prejudice or disclaimer; and in light of the canceling of these claims, dependencies of various of the remaining claims have been amended.

Moreover, new claims 21-26 have been added to the application. Claims 21 and 22, respectively dependent on each of the device claims and on each of the wafer claims, define the side planes of the various structures as forming peripheral edges of the recited structure. Claims 23 and 24, dependent respectively on any one of claims 2, 3 and 9 and on claim 4, each recites that the stress relaxing layer is adhered to the semiconductor device by an adhesion layer, with a linear expansion coefficient of the organic protecting film being substantially equivalent to the linear expansion coefficient of the adhesion layer.

Claims 25 and 26, each dependent on any one of claims 2, 3 and 9, respectively recites that the porous stress relaxing layer has a greater porosity than that of the organic protecting film; and recites that the organic protecting film is colored black.

As for the claim amendments and new claims, see, e.g., pages 6-10 of Applicants' Substitute Specification submitted with the Preliminary Amendment filed March 31, 2000.

The restriction requirement as set forth in Items 2-7 of the Office Action mailed September 13, 2001, is noted. Applicants respectfully affirm their election of the Group I claims, claims 1-17 and 20. It is respectfully submitted that, of the claims remaining in the application, claims 2-6, 9-14, 17 and 20-26 fall within the elected group.

Non-elected claims 18 and 19 are being maintained in the present application, subject to the filing of a Divisional application directed to the subject matter thereof.

The objection to claim 17 on the basis that the word "are" should be deleted from line 10 thereof, is noted. In view of the present amendments to claim 17, the required amendment of line 10 of claim 17 has been satisfied.

Rejection of claims 2-9 and 20 under the second paragraph of 35 USC 112, as being indefinite, set forth in Items 10 and 11 on page 3 of the Office Action mailed September 13, 2001, is noted. Applicants have amended claims 2,

3 and 9 to further clarify that the various components are exposed outside "of the semiconductor device". Thus, it is respectfully submitted that the claims are sufficiently clear as to what the side planes are "outside of", such that the claims satisfy the second paragraph of 35 USC 112 with respect to this aspect of the present invention.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the references as applied by the Examiner in rejecting the claims considered in the Office Action mailed September 13, 2001, that is, the teachings of the U.S. patents to Feger, et al., No. 6,130,472, to Takenouchi, et al., No. 5,744,758, and to Bruce, et al., No. 6,107,107, under the provisions of 35 USC 102 and 35 USC 103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a semiconductor device, or module having a plurality of such devices, as in the present claims, including, inter alia, wherein side planes of the stress relaxing layer, the semiconductor chip and the organic protecting film are exposed outside of the semiconductor device on a same plane. See claims 2, 3 and 9. See also claim 20.

In addition, it is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a

semiconductor wafer as in the present claims, having a chip for forming a semiconductor device, and having the stress relaxing layer provided on a plane of this chip of this wafer, and also having an organic protecting film provided on the plane opposite to this plane on which the stress relaxing layer is provided, with side planes of the stress relaxing layer being exposed to outside of the semiconductor device. Note claims 10, 11 and 17.

Furthermore, it is respectfully submitted that these references would have neither taught nor would have suggested such device, or such wafer, as in the present claims, wherein these side planes, which are exposed outside of the semiconductor device, form a peripheral edge of the respective structures. See, for example, claims 21 and 22.

Moreover, it is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a semiconductor device as in the present claims, including the stress relaxing layer, chip and organic protecting film as discussed previously, and wherein the organic protecting film has a linear expansion coefficient equivalent to the linear expansion coefficient of the stress relaxing layer (note claim 4), and/or wherein the stress relaxing layer is adhered to the semiconductor chip by an adhesion layer, with a linear expansion coefficient of the organic protecting film being substantially equivalent to the linear expansion coefficient of the adhesion layer (see claim 23; note also claim 24).

Furthermore, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested such a semiconductor device as in the present claims, and including additional aspects of the present invention as in the remaining, dependent claims, including (but not limited to) wherein the porous stress relaxing layer has a greater porosity than that of the organic protecting film (see claim 25); and/or wherein the organic protecting film is colored black (see claim 26).

The present invention as claimed in the above-identified application is directed to a semiconductor device having a chip size package of the type used for a high density mounting module, and a multichip module utilizing such semiconductor device.

A chip size package (CSP) manufactured by steps of forming bumps on a wafer, connecting the wafer with a substrate, sealing the interval between the substrate and wafer with a resin, forming external electrodes, and cutting the wafer into respective devices, has a problem of warping of the wafer and semiconductor device due to curing shrinkage, because the resin layer was formed on only one side of the wafer. Additionally, many of the CSPs have an exposed plane, which is opposite to the plane whereon the circuits are formed on the chip. Therefore, there is a problem in that failures, such as cracks, were generated at the edge of the chip, and damage to the rear plane occurred due to the package falling down during transportation and handling, such as when the

package is picked up during a mounting operation.

An additional problem arising in connection with CSPs, using a resin substrate, is that water absorbed in the package expanded, e.g., at re-flow, and failures, such as bubble formation and peeling, occurred.

Against this background, Applicants provide structure which avoids the foregoing problems, the structure in particular avoiding problems due to moisture and breakage, as well as avoiding warping. Applicants have found that by utilizing a porous stress relaxing layer which is exposed to the outside of the semiconductor device, this stress relaxing layer being used together with the organic protecting film provided on an opposite side of the chip to that provided with the stress relaxing layer, objectives according to the present invention are achieved. Specifically, by utilizing a porous stress relaxing layer, with side planes thereof exposed outside of the semiconductor device, moisture absorbed can be released outside of the package through the porous stress relaxing layer, thereby avoiding possible cracking and peeling due to, e.g., expansion of the moisture at mounting re-flow.

In addition, by utilizing the porous stress relaxing layer and organic protecting film on opposite sides of the chip, with the side planes and the various structures exposed to outside of the semiconductor device on a same plane, damage due to expanding moisture upon re-flow can be avoided, as discussed previously; and, moreover, warping of the device, or cracking where the device

is dropped, can be avoided. In this regard, through exposure of the various structures outside of the semiconductor device on the same plane, as in various of the present claims, damage to edge portions of the chips and cracks are scarcely generated.

Furthermore, according to the present invention having the exposed side planes, the wafer, stress relaxing layer and organic protecting film, as well as, e.g., the circuit layer, can be cut simultaneously along a same plane to form respective units, simplifying the processing. In addition, any difference in package area relative to chip area can be reduced, because the wafer, stress relaxing layer and circuit layer can be cut simultaneously along a same plane to form respective units.

As to advantages according to the present invention, note, for example, from page 47, line 9 to page 48, line 17, of Applicants' Substitute Specification submitted with the Preliminary Amendment filed March 31, 2000 in the above-identified application.

Feger, et al. discloses moisture and/or ion barriers that are capable of protecting silicon devices and wiring, for example, copper wiring, found in chip level interconnects, from moisture and/or ions. The barriers are made of polymeric compounds such as hydrocarbons and fluoropolymers as a moisture and/or ion barrier layer. This patent discloses that the polymeric barrier layer can be used for front side as well as back side protection of silicon devices.

Note column 1, lines 8-16 and 20-22. Note also column 3, lines 16-29. Note further column 4, lines 33-37, 40-43 and 49-54. See also column 5, lines 46-50 and 54-58. See also column 6, lines 25-30 and 60-62.

It is emphasized that the concern of Feger, et al. is to provide moisture/ion barriers, for inhibiting the penetration of moisture and/or ions from coming into contact with the metal wiring found in chip level interconnects. It is respectfully submitted that this disclosure of Feger, et al. would have neither taught nor would have suggested, and in fact would have taught away from, the presently claimed subject matter, including the exposed side planes, especially exposed side planes of porous material.

Note also the paragraph bridging columns 2 and 3 of Feger, et al., which discloses that if the barrier is applied after the chips are diced from the wafer, the moisture/barrier layer can protect the side walls of the diced edge. It is respectfully submitted that taking the teachings of Feger, et al. as a whole, including its intended purpose, this patent would have taught away from the present invention of the exposed structure outside of the semiconductor device.

Moreover, it is respectfully submitted that any modification of Feger, et al., for exposing structure corresponding to that as in the present invention, is contrary to the purpose of Feger, et al. Accordingly, such modification would clearly be improper. See In re Ratti, 123 USPQ 349 (CCPA 1959).

Moreover, it is respectfully submitted that the teachings of Feger, et al.

would have neither taught nor would have suggested the other aspects of the present invention, as set forth in the remainder of Applicants' claims and as discussed in the foregoing.

It is respectfully submitted that the secondary references applied by the Examiner, Bruce, et al. and Takenouchi, et al., would not have rectified the deficiencies of Feger, et al. such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Thus, Takenouchi, et al. discloses a multilayer circuit board having a plurality of thermosetting resin films, each carrying circuit patterns, layered with each other. The multilayer circuit board is described most generally in the paragraph bridging columns 2 and 3 of this patent. Note also column 4, lines 55-58, and column 6, lines 35-44.

Initially, it is noted that Takenouchi, et al. is directed to a multilayer circuit board. It is respectfully submitted that one of ordinary skill in the art concerned with in Feger, et al., involving chip level interconnects and moisture/ion barrier layers for chip packages, would not have looked to the teachings of Takenouchi, et al. That is, in view of the different technologies involved in connection with Feger, et al. and Takenouchi, et al., and different problems addressed by each, these patents are directed to non-analogous arts, such that one of ordinary skill in the art concerned with in Feger, et al. would not have looked to the teachings of Takenouchi, et al.

In addition, it is respectfully submitted that the Examiner has pointed to no proper motivation for combining the teachings of Feger, et al. with the teachings of Bruce, et al. Absent such motivation, clearly the combining of the teachings of the references is improper.

In any event, even assuming, arguendo, that the teachings of Feger, et al. and Takenouchi, et al. were properly combinable, such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including exposure of side planes of the various structure to the outside of the semiconductor device; and/or wherein various structure have their side planes in a same plane, or other aspects of the present invention as discussed in the foregoing, and advantages achieved by the present invention.

Bruce, et al. discloses failure analysis and fault isolation techniques employed in cases where the front side surfaces of integrated circuits are inaccessible, or where several layers of metal interconnects prevent the use of more conventional circuit probing techniques upon the front side surface. See column 1, lines 11-16. The technique in Bruce, et al. provides an antireflective coating material onto the back side surface of the substrate prior to detecting electromagnetic radiation emanating from the back side surface, the layer of antireflective coating material reducing reflections which contribute to background noise levels; as a result of the reduced background noise levels, detection capabilities of the methods and the resolutions of any scanned images

produced using the methods are improved. See column 4, lines 42-54.

It is respectfully submitted that Bruce, et al. and Feger, et al. are directed to different technologies, and address different problems. Accordingly, it is respectfully submitted that these references are directed to non-analogous arts, and that one of ordinary skill in the art concerned with in Feger, et al. (providing chip level interconnects) would not have looked to the teachings of Bruce, et al. (analyzing electronic circuits from the back side surface of the substrate).

Furthermore, it is respectfully submitted that the Examiner has pointed to no proper motivation for combining the teachings of Bruce, et al. with the teachings of Feger, et al., as applied by the Examiner.

In any event, even assuming, arguendo, that the teachings of Bruce, et al. were properly combinable with the teachings of Feger, et al., such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including exposing the specified structure to outside of the semiconductor device, according to the present invention which uses a porous stress relaxing layer, much less wherein the side planes of the various structure are exposed to the outside in a same plane, or other aspects of the present invention as discussed in the foregoing, and advantages of the present invention.

Furthermore, it is respectfully submitted that the combined teachings of all three of Feger, et al., Bruce, et al. and Takenouchi, et al., would have neither

taught nor would have suggested the present invention. As discussed previously, it is respectfully submitted that each of Takenouchi, et al. and Bruce, et al. constitute non-analogous art with respect to the subject matter of Feger, et al., such that one of ordinary skill in the art concerned with in Feger, et al. would not have looked to the teachings of Takenouchi, et al. or Bruce, et al.; and, moreover, there has not been established any proper motivation for combining the teachings of both of Takenouchi, et al. and Bruce, et al. with the teachings of Feger, et al.

In any event, even assuming, arguendo, that the teachings of these three references were properly combinable, such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including exposure of side planes of the specified structure, utilizing the porous stress relaxing layer, much less wherein the side planes are in a same plane, or other aspects of the present invention and advantages thereof.

The contention by the Examiner that Feger, et al. discloses the side planes of the chip and porous layer being exposed outside, is respectfully traversed. It is respectfully submitted that the purpose of Feger, et al. is to avoid such exposure. That is, providing such exposure would destroy Feger, et al. for its intended purpose, of providing moisture/ion barrier layers. Such modification of Feger, et al., destroying the reference for its intended purpose, is improper under the requirements of 35 USC 103. See In re Ratti, supra.

Furthermore, it is respectfully submitted that Feger, et al. is silent with respect to side planes of the various components being in a same plane, as in various of the present claims, and advantages of this structure as discussed previously.

In view of the foregoing comments and amendments to the claims, reconsideration and allowance of all claims remaining in the application are respectfully requested.

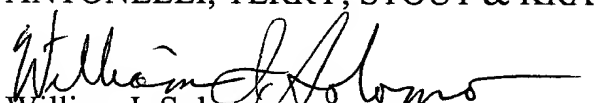
Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. This marked-up version is on the attached pages, the first page of which is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the

filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 503.37770X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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